## CLAIMS

What is claimed is:

1. A processor having a memory interface comprising:

a multi-stage pipeline for fetching or reading information from a memory coupled to the processor, the pipeline including:

a read stage to read a unit of information from the memory;

a correction stage to correct a soft error detected in a read unit of information; and

a utilization stage to utilize information in the corrected information.

2. The processor of claim 1

wherein the read stage comprises an instruction read stage to read a program instruction unit of information from the memory,

wherein the correction stage comprises an instruction correction stage to correct a detected soft error in the read instruction, and

wherein the utilization stage comprises an instruction decode stage to decode the corrected instruction unit of information.

3. The processor of claim 1

wherein the read stage comprises an instruction read stage to read a program instruction unit of information from the memory,

wherein the correction stage comprises an instruction correction stage to correct a detected soft error in the read instruction, and

wherein the utilization stage comprises an instruction execution stage to execute the corrected instruction unit of information.

4. The processor of claim 1

wherein the read stage comprises a data read stage to read a data unit of information from the memory,

wherein the correction stage comprises a data correction stage to correct a detected soft error in the read data, and

wherein the decode stage comprises a data decode stage to decode the corrected data unit of information.

5. The processor of claim 1 wherein the read stage is adapted to read a previously stored unit of information from the memory and an associated error correction code previously stored in the memory.

6. The processor of claim 5 wherein the previously stored unit of information is 32 bits and the previously stored error correction code is a 6 bit Hamming code.

7. The processor of claim 1 wherein the read stage and the correction stage are both operable within a single cycle of the attached memory.

8. The processor of claim 1 further comprising:
control logic to enable and disable operation of the correction stage.

9. The processor of claim 1 further comprising:
correction logic to write the corrected data back to the memory; and
notification logic coupled to the correction logic to signal correction the correction logic that corrected data is available.

10. The processor of claim 9 wherein the notification logic includes:
error storage for storing the address of the corrected data in the memory.

11. The processor of claim 10 wherein the error storage further includes:
error data storage for storing the erroneous value read from the memory.

12. The processor of claim 1 wherein the multi-stage pipeline further comprises:
a write correction stage to write corrected data back to the memory.

13. The processor of claim 9 wherein the correction logic is implemented as programmed instructions to be executed by the processor.

14. The processor of claim 13 wherein the notification logic is adapted to generate an interrupt signal in the processor and wherein the correction logic is executed in response to detection of the interrupt signal.

15. The processor of claim 1 wherein the correction stage is operable within a single cycle of the attached memory.

16. The processor of claim 1 wherein correction of a soft error requires more than a single cycle of the attached memory and wherein the pipeline further includes:

multiple correction stages to correct a soft error detected in a read unit of information.

17. A method for correcting soft errors in a pipelined processor coupled to a memory subsystem, the method comprising:

reading a unit of information from an attached memory in a read stage of the processor pipeline;

correcting a soft error in the read information in a correction stage of the processor pipeline; and

utilizing the corrected information in a utilization stage of the processor pipeline.

18. The method of claim 17 wherein the step of correcting comprises:

correcting the read information in multiple correction stages of the processor pipeline.

19. The method of claim 17 wherein the steps of correcting and utilizing are performed within a single memory cycle of an attached memory system.

20. The method of claim 17 further comprising:

selectively disabling operation of the correction stage.

21. The method of claim 17 wherein the step of reading comprises:

reading a unit of data; and

reading a corresponding error correcting code previously stored with the unit of data.

22. The method of claim 21

wherein the step of reading a unit of data comprises reading a 32 bit data value, and

wherein the step of reading a corresponding error correcting code comprises reading a 6 bit Hamming code.

23. The method of claim 17 further comprising:

storing information regarding a soft error corrected in the step of correcting.

24. The method of claim 23 wherein the step of storing comprises:

saving an address value of the location that provided the corrected soft error.

25. The method of claim 24 wherein the step of storing further comprises:

saving an erroneous data value that provided the corrected soft error.

26. The method of claim 17 further comprising:

notifying the processor that a soft error was corrected.

27. The method of claim 26 further comprising:

executing instructions in the processor to write the corrected information into the memory.

28. The method of claim 26 wherein the step of notifying comprises:

interrupting the processor to signal correction of a soft error.

29. The method of claim 17 further comprising:

writing the corrected information to the memory in a write corrected information stage of the processor pipeline.